circuit on the semiconductor substrate.

Cancel Claims 38 and 39.

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The Examiner considered the arguments presented in the Amendment After Final filed on November 28, 2001, but was not persuaded. In the Amendment After Final, dependent Claims 38 and 39 were canceled to address the Examiner's rejection thereof. Since the Amendment After Final was not entered by the Examiner, these claims are being canceled herein.

In addition, independent Claims 9, 15, 21, 29 and 36 are being amended herein to more clearly define the present invention over the cited prior art references. In particular, the independent claims are being amended to recite that the voltage ramp generator is an integrated circuit voltage ramp generator formed on a semiconductor substrate. Support in the specification is found on page 4, lines 26-31. The dependent claims have been amended for consistency. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached paper is captioned "Version With Markings to Show Changes Made."

The Examiner rejected independent Claims 9, 15, 21, 29 and 36 over the Tanigawa patent in view of the Applicants' prior art FIG. 1. The Examiner cited the Applicants' prior art FIG. 1 as disclosing a ramp generator having a current source Ig1 with no expressed teaching of the structure thereof. The Examiner cited Tanigawa as disclosing in FIG. 4

a current sink comprising "a current mirror" which has the advantage of gain control.

The Examiner has taken the position that it would have been obvious to modify the current sink as disclosed in Tanigawa to a current source, and replace the current source Ig1 in the Applicants' prior art FIG. 1 with the modified current source. Moreover, the Examiner has further taken the position that since this modification yields a circuit identical in structure to the claimed invention, "it must inherently have the same function."

The claimed invention, as recited in amended independent Claim 9, for example, is directed to an integrated circuit voltage ramp generator comprising a semiconductor substrate, a capacitance on the semiconductor substrate, and a charging circuit on the semiconductor substrate and connected to the capacitance. The charging circuit comprises a current generator having a first resistance, and a circuit connected to the current generator and to the capacitance. The charging circuit has a second resistance. The charging circuit enables a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance.

Independent Claim 9 has been amended so that the voltage ramp generator more clearly defines over the Tanigawa patent in view of the Applicants' prior art FIG. 1. In other words, the voltage ramp generator is an integrated circuit voltage ramp generator formed on a semiconductor substrate. In Tanigawa, the gain control device illustrated in FIG. 4 is not suitable for semiconductor circuit integration. Reference is directed to column 1, line 65 through column 2, line 2 in Tanigawa, which provides:

> "However, since the variable resistor R is necessary to be connected to the emitter of the transistor Q2 externally in the circuit shown in FIG. 4, an external leading terminal is required. Accordingly, the circuit of FIG. 4, as it is, is not suitable for semiconductor circuit integration." (Emphasis added.)

Therefore, even if the references were combined as suggested by the Examiner, the claimed invention is not produced. In fact, Tanigawa teaches away from the claimed invention since the circuit illustrated in FIG. 4 is not suitable for semiconductor circuit integration.

Yet another distinction of the claimed invention over the Tanigawa patent in view of the Applicants' prior art FIG. 1 is with respect to the capacitance charging current being controlled based upon the ratio of the second and first resistances. In particular, the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

The second resistance in the claimed invention advantageously permits compensation for a spread of the first resistance. This spread may be due to operating temperature changes, for example. Without the second resistance, the spread of the first resistance is reflected in variations of the capacitance charging current. Therefore, to compensate for the spread of the first resistance, the second resistance is included.

In reference to the current ramp generator illustrated in the Applicant' prior art FIG. 1, the spread of resistances Rg1 and Rs cause the current ramp to vary. The resistance Rg1 is the resistance of the current generator

connected to the capacitance C. The resistances Rg1 and Rs can have a spread on the order of $\pm$ 20%, for example. These spreads are then reflected in the generated current ramp on the order of $\pm$ 40%, for example, as discussed on page 3, lines 9-14 in the Applicants' specification. Adjustment of the current ramp spread in the current ramp generator illustrated in the Applicant' prior art FIG. 1 is accomplished by adjusting the resistance Rs with fuse type memory points. The resistance Rs is thus produced as a combination of fuses to obtain the desired resistance.

Referring again to FIG. 4 of the Tanigawa patent, the relationship between the signal current I_1 of the gain control circuit and the output current I_2 is based upon the equation $I_2 = I_1 * A$. In the Amendment After Final, the Applicants' characterized the output current I_2 as the capacitance charging current. Tanigawa discloses that the variable A is based upon the equation $\exp(V_{BE}/V_T)$, with V_T being a thermal voltage. Referring to column 1, lines 59-61 in Tanigawa, which provides:

> "Therefore, the output current I_2 is set equal to a value A times larger than the input current I_1 ..." (Emphasis added.)

Tanigawa further discloses that by changing the value of the variable resistance R, the voltage thereacross is varied so that the gain of the gain control circuit can be set to a desired value.

In the Amendment After Final, the Applicants' argued that even if the references were combined as suggested by the Examiner, the claimed invention is not produced. The Applicants' prior art FIG. 1 and the Tanigawa patent both fail

to teach or suggest that the capacitance charging current is proportional to a square of a ratio of the second resistance (from Tanigawa) and the first resistance (internal resistance of current source Ig1 in the Applicants' prior art FIG. 1), as recited in independent Claim 9, for example.

In paragraph 5 of the Advisory Action, the Examiner states that this argument only deals with the steady-state operation of the gain control device illustrated in FIG. 4 of Tanigawa. The Examiner further states that this has nothing to do with the charging current that will exist when FIG. 4 is combined with the Applicants' prior art FIG. 1. However, in the discussion of FIG. 1 provided in the Background Section of the Applicants' specification, there is no reference that the capacitance charging current should be proportional to a square of a ratio of two different resistances, as recited in the claims.

It thus appears that the Examiner is using impermissible hindsight reconstruction to modify Tanigawa in view of the Applicants' prior art FIG. 1 in an attempt to produce the claimed invention. The prior art references, individually or in combination, do not teach or suggest that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance. As discussed above, FIG. 4 of the Tanigawa patent even teaches away from the claimed invention because it is not suitable for semiconductor circuit integration.

Accordingly, it is submitted that amended independent Claim 9 is patentable over Tanigawa in view of the Applicants' prior art FIG. 1. Amended independent Claims 15, 21, 29 and 36 are similar to amended independent Claim 9 by also reciting that the voltage ramp generator is an integrated

circuit voltage ramp generator formed on a semiconductor substrate, and that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

In view of the patentability of the independent claims as discussed above, it is submitted that their dependent claims, which recite yet further distinguishing features, are also patentable over the prior art. Thus, these dependent claims require no further discussion herein.

In view of the amendments and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

9. (Twice Amended) [A] An integrated circuit voltage ramp generator comprising:

a semiconductor substrate;

a capacitance on said semiconductor substrate; and

a charging circuit on said semiconductor substrate and connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance.

10. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 9, wherein said charging circuit comprises a degenerate current mirror circuit.

11. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 10, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

12. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 11, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

13. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 9, wherein said capacitance comprises a gate capacitance of a MOS transistor.

14. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 9, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

15. (Twice Amended) [A] An integrated circuit voltage ramp generator comprising:

a semiconductor substrate;

a capacitance on said semiconductor substrate; and

a charging circuit on said semiconductor substrate and connected to said capacitance and comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance.

17. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 15, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

18. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 17, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

19. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 15, wherein said capacitance comprises a gate capacitance of a MOS transistor.

20. (Amended) [A] An integrated circuit voltage ramp generator according to Claim 15, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

21. (Twice Amended) [A] An integrated circuit current ramp generator comprising:

a semiconductor substrate;

a voltage ramp generator on said semiconductor substrate and comprising

a capacitance, and

a charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance having a

second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

a conversion circuit on said semiconductor substrate and connected to said voltage ramp generator for generating a current ramp.

22. (Amended) [A] An integrated circuit current ramp generator according to Claim 21, wherein said conversion circuit comprises a third resistance.

23. (Amended) [A] An integrated circuit current ramp generator according to Claim 21, wherein said third resistance comprises an implanted resistance having a positive temperature coefficient.

24. (Amended) [A] An integrated circuit current ramp generator according to Claim 21, wherein said charging circuit comprises a degenerate current mirror circuit on said semiconductor substrate.

25. (Amended) [A] An integrated circuit current ramp generator according to Claim 24, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a

source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

26. (Amended) [A] An integrated circuit current ramp generator according to Claim 25, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

27. (Amended) [A] An integrated circuit current ramp generator according to Claim 21, wherein said capacitance comprises a gate capacitance of a MOS transistor.

28. (Amended) [A] An integrated circuit current ramp generator according to Claim 21, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

29. (Twice Amended) [A] An integrated circuit current ramp generator comprising:

a semiconductor substrate;

a voltage ramp generator on said semiconductor substrate and comprising

a capacitance having a first resistance, and

a charging circuit connected to said capacitance and comprising

a current generator, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance; and

a third resistance on said semiconductor substrate and connected to said voltage ramp generator for generating a current ramp.

31. (Amended) [A] An integrated circuit current ramp generator according to Claim 29, wherein said third resistance comprises an implanted resistance having a positive temperature coefficient.

32. (Amended) [A] An integrated circuit current ramp generator according to Claim 29, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a

source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

33. (Amended) [A] An integrated circuit current ramp generator according to Claim 32, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

34. (Amended) [A] An integrated circuit current ramp generator according to Claim 29, wherein said capacitance comprises a gate capacitance of a MOS transistor.

35. (Amended) [A] An integrated circuit current ramp generator according to Claim 29, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

36. (Twice Amended) A method for generating a ramp voltage comprising [the steps of]:

generating a capacitance charging current using [a] an integrated circuit charging circuit comprising a semiconductor substrate, and a current generator on the semiconductor substrate and having a first resistance and a circuit on the semiconductor substrate and connected to the generator having a second resistance for enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

charging a capacitance on the semiconductor substrate with the capacitance charging current for generating the ramp voltage.

37. (Amended) A method according to Claim 36, wherein the circuit comprises a degenerate current mirror circuit on the semiconductor substrate.

Claims 38 and 39 have been cancelled.